**Challenge of Applying Ohmic Contacts to Gallium Arsenide Devices: In-Depth Look**

Metal-to-semiconductor (M-S) contacts are present in every semiconductor device. Low-resistance, stable contacts are critical for the performance and reliability of integrated circuits, and their preparation and characterization are major efforts in circuit fabrication. They can behave either as a Schottky barrier, or as an ohmic contact, depending on the characteristics of the interface. They can behave either as a Schottky barrier, or as an ohmic contact, depending on the characteristics of the interface. Schottky barriers act as rectifiers (diode-like), while ohmic contacts provide current linear with applied voltage (i.e., constant resistance) and are considered “transparent.” Application of ohmic contacts to compound semiconductors is considerably more difficult than with silicon or germanium. Methods and materials for achieving ohmic contacts to gallium arsenide (GaAs) will be described in the following.

## Introduction - Metal-Semiconductor Junctions

A wide range of metals, such as silver (Ag), gold (Au), copper (Cu), aluminum (Al) and alloys are used to make electrical contacts to semiconductors. The behavior of the junctions depends on the energy band structures and the work functions of the constituent materials. When in thermal equilibrium, and in the absence of an applied electric field, the Fermi levels (i.e., electrochemical potential) of any two solids in contact with each other must align. In this case, the Fermi levels of the metal and semiconductor must align. The work function ($\Phi$) of the material is the difference between the Fermi energy ($E_F$) and vacuum level; the energy needed to remove an electron to infinity [1,2]. The contacting metal and semiconductor will generally have different work functions, $\Phi_M$ and $\Phi_S$ respectively.

Table 1 shows work functions of a variety of metals. When the two materials are placed in contact, electrons will flow from the one with the lower work function to the one with the higher work function until the Fermi levels equilibrate (align). As a result, the material with the lower work function will take on a slight positive charge, while that with the higher work function will become slightly negative.

As with any band bending behavior, there is a built-in potential ($V_{bi}$) associated with the contact between two materials. $V_{bi}$ is the root cause for rectification in diodes. We are concerned here with band bending at the S-M interface. The goal is to reduce band bending and work function differences to achieve ohmic behavior and “free” movement of charge carriers across the junction.

Table 1. Work Functions of Selected Metals [1]

| Material | Face | W (eV) | IE(1) (eV) |
|---|---|---|---|
| Li | Polycrystal | 2.90 | 5.39 |
| Na | Polycrystal | 2.75 | 5.14 |
| K | Polycrystal | 2.30 | 4.34 |
| Rb | Polycrystal | 2.16 | 4.18 |
| Cs | Polycrystal | 2.14 | 3.89 |
| Al | (100) | 4.41 | 5.99 |
| | (110) | 4.06 | 5.99 |
| | (111) | 4.24 | 5.99 |
| Ag | (100) | 4.64 | 7.58 |
| | (110) | 4.52 | 7.58 |
| | (111) | 4.74 | 7.58 |
| Cu | (100) | 4.59 | 7.48 |
| | (110) | 4.48 | 7.48 |
| | (111) | 4.98 | 7.48 |
| Au | (100) | 5.47 | 9.23 |
| | (110) | 5.37 | 9.23 |
| | (111) | 5.31 | 9.23 |
| W | (100) | 4.63 | 7.98 |
| | (110) | 5.25 | 7.98 |
| | (111) | 4.47 | 7.98 |
| Ni | (100) | 5.22 | 7.64 |
| | (110) | 5.04 | 7.64 |
| | (111) | 5.35 | 7.64 |
| Mo | (100) | 4.53 | 7.10 |
| | (110) | 4.95 | 7.10 |
| | (111) | 4.55 | 7.10 |

## Schottky Barrier and Ohmic Contacts

Figure 1 shows a typical M-S junction [3]. It consists of a metal contacting a semiconductor surface, or junction. An ideal ohmic contact, a contact in which no potential exists between the metal and the semiconductor, is made to the other side of the semiconductor. The sign convention of the applied voltage and current is also shown in Figure 1. We can now view the M-S contact in more detail.

Figure 2 shows the relationship between energy bands and work functions for metal and semiconductor. The barrier between the metal and the semiconductor can be identified on an energy band diagram. To construct such a diagram, we first must consider the energy band diagram of the metal and the semiconductor, and align them using the same vacuum level as depicted in Figure 2.

Figure 2A shows the work function of the metal with respect to the Fermi level. Figure 2B shows the work function of a p-type semiconductor, including the conduction band valence band, Fermi level and electron affinity (⍰$_S$). Figure 2C shows the energy is the sum of $V_{bi}$ and the offset between $E_F$ and the conduction band (CB). For n-type semiconductors:band structure

at the S-M junction. Ignoring quantum mechanics, the Schottky-Mott theory informs us that in order to surmount the barrier, a carrier in the semiconductor must gain enough energy to jump from the Fermi level ($E_F$) to the top of the bent conduction band. The energy ($\square_B$) required

$$\square_B = \square_M - \square_S$$

Here the electron affinity $\square_S$ is defined as the energy difference between the vacuum level and the CB level. For p-type materials:

$$\square_B = E_g - (\square_M - \square_S) \quad \text{Where } E_g \text{ is the bandgap.}$$

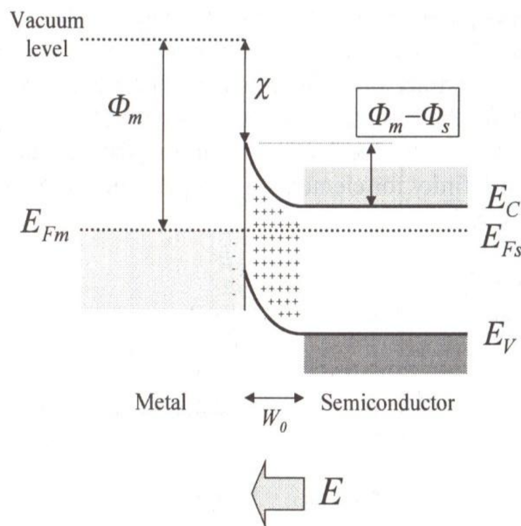



Figure1. Metal-Semiconductor Junction [3]

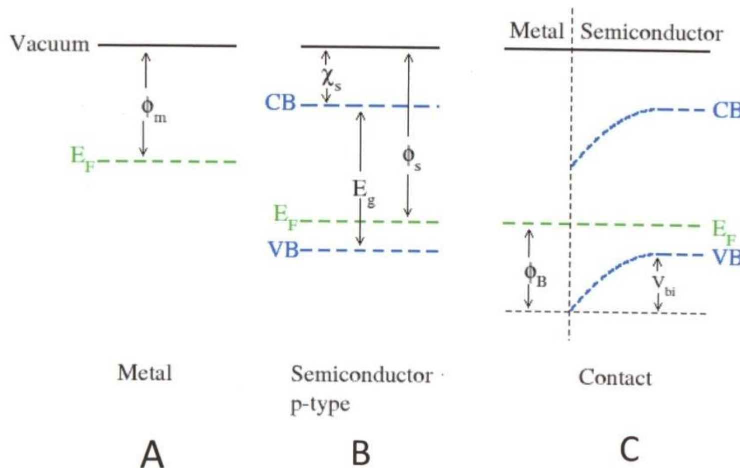



Figure 2. Elements of Metal and Semiconductor Forming a Semiconductor-Metal Junction (left)

Charge transfer is at the root of energy band shifting. Since overall charge neutrality must be maintained when a metal and semiconductor are brought together, excess electrical charges inside the semiconductor and those inside the metal must be equal but opposite [3]. Thus, the degree of band bending and direction of electron transfer depend on the difference between $\square_M$ and $\square_S$.

Figure 3 refers to an n-type semiconductor, if $\Phi_M < \Phi_S$ energy bands in the semiconductor shift downward by $\Phi_B$ in order to align the Fermi energy on both sides of the junction. However, Figure 4 shows if $\Phi_M > \Phi_S$ energy bands of the semiconductor actually shift upward with respect to those of the metal. Signs of the charge carriers which appear on either side of the junction and the direction of the built-in electric field are also shown in the Figure. The built-in electric field forms in exactly the same manner as a p-n junction (discussed in a previous article). For p-type semiconductors, if $\Phi_M < \Phi_S$, energy bands in the semiconductor shift upward with respect to those of the metal.

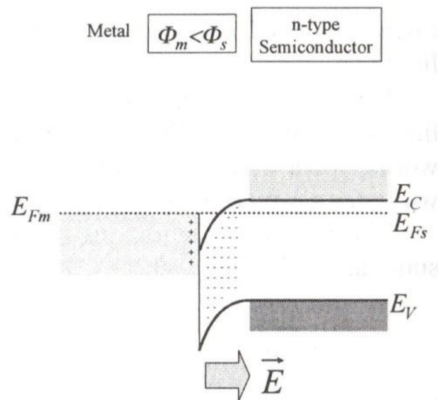



Figure 3. Shift in Energy Bands in a M-S Junction When $\Phi_M < \Phi_S$ [3]

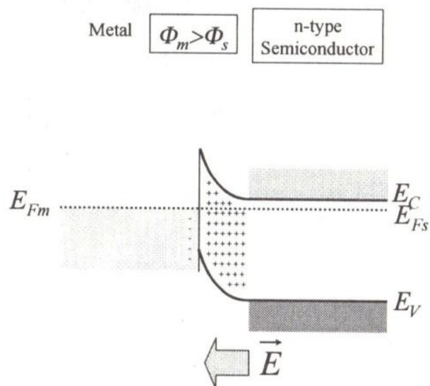


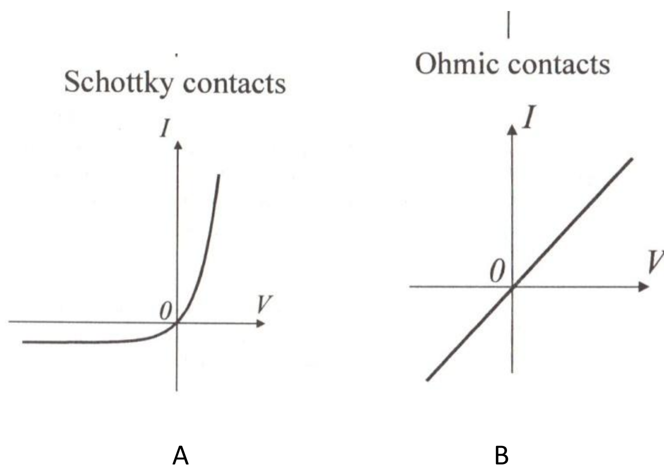

Figure 4. Shift in Energy Bands in a M-S Junction When $\Phi_M > \Phi_S$ [3]

The electrical properties of a M-S junction depend on whether or not the depletion region is created as a result of charge redistribution, which in turn depends on the $\Phi_M - \Phi_S$ and the type of semiconductor (i.e., n-type or p-type). As already addressed, electrons move from the semiconductor to the metal when $\Phi_M > \Phi_S$. The type of semiconductor now becomes important in determining the type of contact (Schottky or ohmic). For n-type semiconductors, electron extraction depletes the semiconductor of its majority charge carriers (electrons). This places the depletion region near the junction and diode, and rectification behavior results, as shown in Figure 5A.

Figure 5B shows I-V characteristics of an ohmic contact. If the semiconductor is p-type, electrons from the semiconductor cause the p-dopants to become ionized, which create more holes (majority charge carriers) and no depletion region is then formed at the junction. As a result, *electrons are free to flow in either direction under an external electric field and the contact formed is ohmic.* Figure 6 shows junctions for p-type semiconductors. Simply put, ohmic junctions are formed in the absence of a depletion region and Schottky junctions are formed in the presence of a depletion region. Table 2 summarizes these concepts.

Table 2. Four Possible Metal-Semiconductor Junction Configurations and the Resulting Contact Type [3]

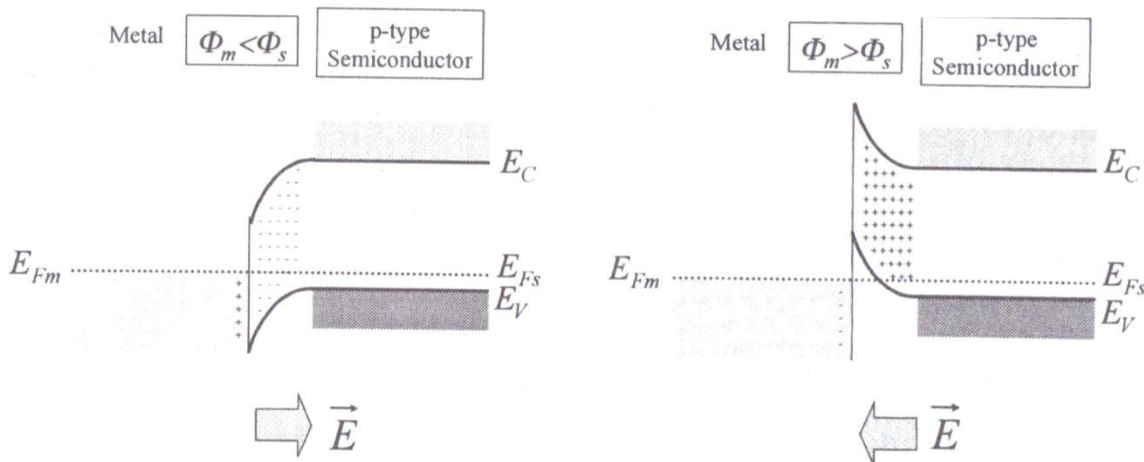
| **Junction Configuration** | **Semiconductor** | **Junction** |
|---|---|---|
| $\Phi_M > \Phi_S$ | n-type | Schottly |
| $\Phi_M < \Phi_S$ | p-type | Schottky |
| $\Phi_M > \Phi_S$ | p-type | ohmic |
| $\Phi_M < \Phi_S$ | n-type | ohmic |




A B

Figure 5. Rectifying and Ohmic M-S Junctions [3] (left)

Figure 6. M-S Junctions for P-Type Semiconductors [3] (below)

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functions often form the best contacts to p-type semiconductors while those with low work functions form the best contacts to n-type semiconductors. Unfortunately, experiments have shown that the predictive power of the model doesn't extend much beyond this statement. Under real conditions, contact metals may react with or diffuse into semiconductor surfaces to form a compound with new electronic properties. A contamination layer at the interface may effectively widen the barrier. The surface of the semiconductor may reconstruct leading to a new electronic state. The dependence of contact resistance on the details of the interfacial chemistry is what makes the reproducible fabrication of ohmic contacts a significant manufacturing challenge.

## Ohmic Contacts to Gallium Arsenide

This introduces the problem of making ohmic electrical contacts to gallium arsenide (GaAs) devices. Formation of ohmic contacts to compound semiconductors is considerably more difficult than with silicon or germanium due to the reactivity of their constituents and inter-diffusion with the metal. Metal work functions actually consist of two components, a volume term and a surface dipole term [4]. Similarly, the electron affinity of a semiconductor also contains a surface dipole term. These surface dipole terms are governed by the way the electronic charge is distributed at the surfaces of the solids and are therefore clearly influenced by the quality, surface state and other properties of the surface. It is, however, impossible to separate the volume and the surface contributions from the work function. When a metal and semiconductor are brought into intimate contact, the atomic positions and the charge distributions of the surfaces in touch will change in an unknown way and additionally have some degree of surface interaction.

The simple theory presented above, therefore cannot be expected to explain and predict barrier heights at such interfaces, since it assumes that electron affinities and work functions remain unchanged when contact is made (which is not the case). In an attempt to overcome this problem, it was suggested that the electronegativity of the metal could be used to predict M-S contact performance, rather than its work function [5 - 7]. Although a number of theories and various mechanisms, including electronegativity , have been proposed in the literature [5-11], no definite explanation regarding the properties of M-S contacts precisely has yet emerged. This is likely due to the lack of detailed information on the nature of M-S contacts on the atomic level and differences in deposition techniques for contacts. To this end, we must attempt to choose metals for ohmic contacts based on the above theory and our “best guess.”

Ohmic metal contacts for GaAs are generally deposited by sputtering or evaporation processes and are photolighographically patterned. As described above, ohmic contacts to semiconductors form when the semiconductor is highly doped. High doping will narrow the depletion region at the junction and allow electrons to flow easily in both directions at any potential by tunneling through the barrier. However, it can be seen that heavy doping is not always possible or advantageous, and definitely not the only means to achieve an ohmic contact to GaAs. Table 3 shows typical contact materials for semiconductors.

Table 3. Contact Materials to Common Semiconductors

| **Material** | **Contact Materials** |
|---|---|
| Si | Al, Al-Si, $TiSi_2$, TiN, W, $MoSi_2$, PtSi, $CoSi_2$, $WSi_2$ |
| Ge | In, AuGa, AuSb |
| GaAs | AuGe, PdGe, PdSi, Ti/Pt/Au, NiGeAu, NiGeNiAu |
| GaN | Ti/Al/Ti/Au, Pd/Au |
| InSb | In |
| ZnO | $InSnO_2$ (ITO), Al |
| $CuIn_{1-x}Ga_xSe_2$ (CIGS) | Mo, ITO |
| HgCdTe | In |

Materials for Ohmic Contacts to GaAs

Table 4 shows Schottky barrier heights for 43 metals with n-type GaAs [4]. Contact to GaAs poses several problems. GaAs surfaces tend to lose arsenic, and the trend towards As loss can be considerably exacerbated by the deposition of metal (hence, a diffusion barrier is often used to prevent As loss). In addition, the volatility of As limits the amount of post deposition annealing that GaAs devices will tolerate. Thus, several techniques are used to reduce Schottky barrier height and create ohmic contacts to GaAs:

- Chemical or plasma surface pretreatment [4,12]
- Thin chalcogenide layer [13,14]
- Low band gap alloy buffer layer: Ni/Ge/Ni/Au [4,14]
- Diffusion barrier layer [14,15]
- Hydrogen plasma [16]

One solution for GaAs and other compound semiconductors is to deposit a low bandgap alloy contact layer, such as NiGeAu [14], as opposed to a heavily doped layer. It is known that n-type GaAs has acceptor-like surface states [17]. Here, in order to obtain ohmic contacts, all states should be filled or emptied. There are two ways of accomplishing this, either by heavy doping of the semiconductor layer or by diffusion of metal from contact layer into the semiconductor. Since the level of doping of GaAs during molecular beam epitaxy (MBE) growth is limited, thermal processing of metallic layers, i.e., annealing, plays a crucial role in contact formation. However, it cannot be forgotten that deep diffusion of metal into epitaxial layers can also damage a device. For example, GaAs has a smaller bandgap than AlGaAs, thus a layer of GaAs near its surface can promote ohmic behavior.

Table 4. Schottky Barrier Heights for 43 Metals with N-Type GaAs [4]

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| .62eV<br>12 Mg<br>.64eV | | | | | | $\phi_{b0}^{I-V}$<br>Element<br>$\phi_{b0}^{C-V}$ | | | | | .77eV<br>Al<br>.76eV | Si | P |
| 20 Ca | .71eV<br>Sc<br>.69eV | .83eV<br>Ti<br>.82eV | .80eV<br>V<br>.80eV | .80eV<br>Cr<br>.83eV | .82eV<br>Mn<br>.83eV | .83eV<br>Fe<br>.84eV | .83eV<br>Co<br>.83eV | .83eV<br>Ni<br>.83eV | .99eV<br>Cu<br>.99eV | .81eV<br>Zn<br>.82eV | .59eV<br>Ga<br>.60eV | Ge | As |
| 38 Sr | .71eV<br>Y<br>.70eV | .77eV<br>Zr<br>.77eV | .77eV<br>Nb<br>.79eV | .87eV<br>Mo<br>.87eV | Tc | .86eV<br>Ru<br>.91eV | .89eV<br>Rh<br>.90eV | .93eV<br>Pd<br>.93eV | .99eV<br>Ag<br>.98eV | .82eV<br>Cd<br>.82eV | .67eV<br>In<br>.68eV | .71eV<br>Sn<br>.70eV | .97eV<br>Sb<br>.99eV |
| 56 Ba | La | .81eV<br>72 Hf<br>.82eV | .78eV<br>Ta<br>79eV | .79eV<br>W<br>.81eV | .87eV<br>Re<br>.88eV | Os | .90eV<br>Ir<br>.91eV | .99eV<br>Pt<br>.99eV | .92eV<br>Au<br>.92eV | Hg | Tl | .86eV<br>Pb<br>.86eV | .88eV<br>Bi<br>.89eV |
| 58 Ce | .76eV<br>Pr<br>.75eV | .76eV<br>Nd<br>.75 | Pm | .75eV<br>Sm<br>.74eV | Eu | .75eV<br>Gd<br>.74eV | .75eV<br>Tb<br>.75eV | Dy | .74eV<br>Ho<br>.74eV | .74eV<br>Er<br>.73eV | .72eV<br>Tm<br>.71eV | .67eV<br>Yb<br>.67eV | Lu |

GaAs/AlGaAs Quantum Cascade Lasers

Ohmic contacts to n-type GaAs (n-GaAs) are critical in GaAs/AlGaAs quantum cascade lasers [14]. Quantum cascade lasers (QCLs) are unipolar sources of mid and far infrared radiation (IR) [3]. QCLs require high voltage for device polarization and high current density to achieve the threshold of lasing action. Low resistance ohmic contacts are critical in order to reduce serial resistance for these devices. Furthermore, contacts should be thermally stable and have low diffusion depths into the metal. Diffusion barriers such as Ti or Ni can reduce loss of As during contact formation [14, 15].

A Ni/GeAu/Ni/Au layer is found to significantly decrease contact resistance to n-GaAs to form ohmic contacts. The resistance of contacts (5nm Ni/100nm AuGe/35nm Ni/300nm Au) deposited by e-beam process and thermal evaporation, and by dc magnetron sputtering system, will be compared. The fabrication process for evaporated films consists of cleaning semiconductor samples in dissolvent and wet etching in order to remove the native oxide. Then, the samples are loaded into a vacuum chamber and the metallic layers deposited. Before sputter deposition, n- GaAs wafers are pre-cleaned by four different processes, including plasma etching by $Ar^+$ ions and wet etching. Samples are then annealed in a gas flow furnace in the temperature range from 400 °C to 450 °C, or are processed with rapid thermal annealing (RTA). Long-term thermal stability is investigated by annealing the samples in a gas flow furnace at a temperature of 200 °C for 8 h, 16 h.

Figure 7 shows a TEM picture of Ni/AuGe/Ni/Au contact on n-GaAs [18] and Figure 8 shows the decrease in contact resistance with time at 200 °C. Lowest contact resistance is achieved for sputtered contacts pre-cleaned with $Ar^+$ ions and wet etching. The average specific contact resistance to GaAs achieved using this layer is about $6\times10^{-7}$ Ωcm$^{-2}$ (GaAs:Si $5\times10^{18}$ cm$^{-3}$). Ni placed between AuGe and GaAs is found to be a good diffusion barrier. Preparation of contacts without pretreatment or with wet etching, result in a high specific resistance and poor thermal stability. Thus, we see that a pristine GaAs surface is critical to achieve an ohmic contact.

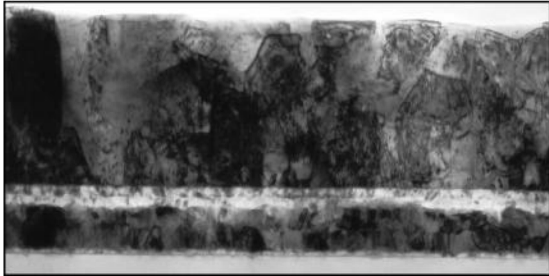

Figure 7. TEM Photo of Ni/AuGe/Ni/Au Contact on N-GaAs [18]. The Bright Band is a Ni Layer.

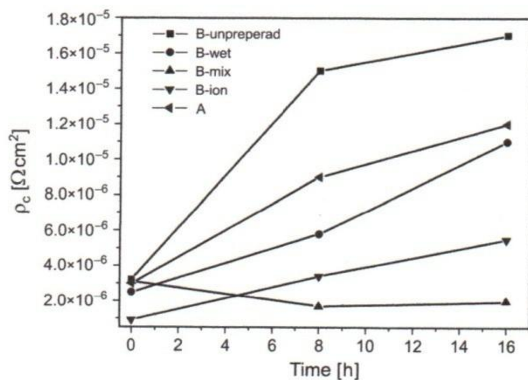


Figure 8. Decrease in Contact Resistance with Time at T = 200°C [18]

Titanium (Ti) is also an effective diffusion barrier [15]. The contact resistance of GeAu/Ni/Ti/Au multilayers to n-GaAs will be compared to that of GeAu/Ni and GeAu/Ni/Au multilayers. All layers are thermally evaporated onto pretreated n-GaAs wafers. Contact resistance of GeAu/Ni/Ti/Au is up to 4.5 times lower that of GeAu/Ni layers and its surface morphology is significantly smoother, as shown in Figure 9.

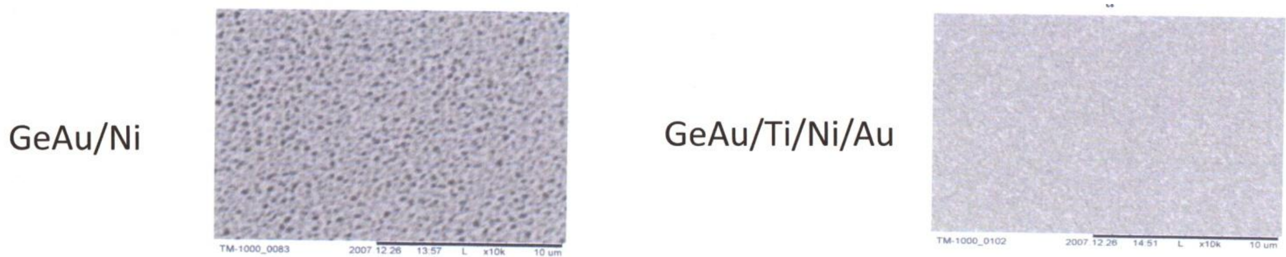


Figure 9. SEM Images of the Ge/Au/Ni (a) and Ge/Au/Ni/Ti/Au (b) Ohmic Contact Pads Surface Produced by Thermal Evaporation and Annealed at 460 °C for 5 Min [15]

Different materials are required for ohmic contacts to p-type GaAs (p-GaAs). Table 5 shows typical

Table 5. Barrier Heights for Contact Metals to P-Type GaAs [19]

| **Metal** | **$\phi_{Bp}$ (eV)<br>p-GaAs** | **$\phi_{Bp}$ (eV)<br>p-$In_{0.52}Ga_{0.47}As$** |
|---|---|---|
| Au | 0.42 – 0.48 | 0.70 |
| Al | 0.61 – 0.65 | |
| Pt | 0.48 | 0.13 |
| Ti | | 0.63 – 0.68 |
| Ni | 0.58 | 0.56 |
| Pd | 0.49 | |

Materion – Supporting the Semiconductor Market

A wide range of metals and semiconductors used in ohmic and Schottky junctions are available from Materion. As a leading high technology company, they can also tailor materials for specific applications for developing ohmic contacts to GaAs and other semiconductor devices. Sputtering and evaporation sources for virtually all contact materials are available from Materion Technical Materials (link to http://materion.com/Businesses/TechnicalMaterials.aspx) while Materion Microelectronics & Services (link to http://materion.com/Businesses/MicroelectronicsandServices.aspx) is a leading supplier of thin film deposition materials for the compound semiconductor market.

In Summary

While a number of materials have been developed for ohmic contacts to n-type and p-type GaAs, multilayers of Ge/Au/Ni, Ni/AuGe/Ni/Au, GeAu/Ni/Au, and GeAu/Ni/Ti/Au appear to possess the lowest contact resistance. One mechanism for this low contact resistance is that Ni and Ti form diffusion barriers to keep the metal from diffusing into the GaAs and forming intermetallics. Rapid thermal annealing and heat treatment at 200°C can also reduce contact resistance.

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